UDIMM DDR4 SDRAM

Rev:1.0

Note:

Company will not give any notice for change of products specifications. This product manual is only for reference. Please contact with Oreton Technology Co., Ltd. for more detail technical parameters and information.

Table of content

1． Product introduction

1.1 Summary

Oreton DDR4 U-DIMM high-speed, memory module that use of 512M x 8 、1024M x 8 、1GX8 、2GX8 bits DDR4 SDRAM in FBGA package and a 4K bits serial EEPROM on a 288-pin printed circuit board. Oreton DDR4 is a Dual In-Line Memory . Module and is intended for mounting into 288-pin edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

1.2 Product model list

Model	Voltage	Capacity	Organization	Data transfer rates	CL
R2666D4P12004G	1.2V	4GB	512Mx8	DDR4-2666	19
R2666D4P12008G	1.2V	8GB	512Mx8	DDR4-2666	19
R2666D4P12008G	1.2V	8GB	1Gx8	DDR4-2666	19
R2666D4P12016G	1.2V	16GB	1Gx8	DDR4-2666	19
R2666D4P12016G	1.2V	16GB	2Gx8	DDR4-2666	19
R3200D4P13508G	1.35V	8GB	1Gx8	DDR4-3200	22
R3200D4P13516G	1.35V	16GB	1Gx8	DDR4-3200	22
R3200D4P13516G	1.35V	16GB	2Gx8	DDR4-3200	22
R3200D4P13532G	1.35V	32GB	2Gx8	DDR4-3200	22

1.3 Specifications

1.3.1 Interface: 288-pin DIMM;

1.3.2 Speed: 2666Mbps,3200Mbps;

1.3.3 Input voltage: DC 1.2V/1.35V (±0.075v);

1.3.4 Operating temperature: 0℃ ~ +85℃;

1.3.5 Storage temperature: -20℃ ~ +100℃;

1.3.6 Physical dimension: 133.35mm length * 31.25mm wide * 4.0mm height error±0.15mm;

1.3.7 Support Capacity: 4GB,8GB,16GB,32GB;

1.3.8 MTBF: one million hours.

1.4 Features

1.4.1 RoHS compliant products;

1.4.2 JEDEC standard 1.2V(1.14V~1.26V) Power supply;

1.4.3. Programmable CAS Latency:10,11,12,13,14,15,16,17,18;

1.4.4 8 bit pre-fetch;

1.4.5 Burst Length (BL) switch on-the-fly BL8 or BC4;

1.4.6 Bi-directional Differential Data-Strobe;

1.4.7 On Die Termination, Nominal, Park, and Dynamic ODT;

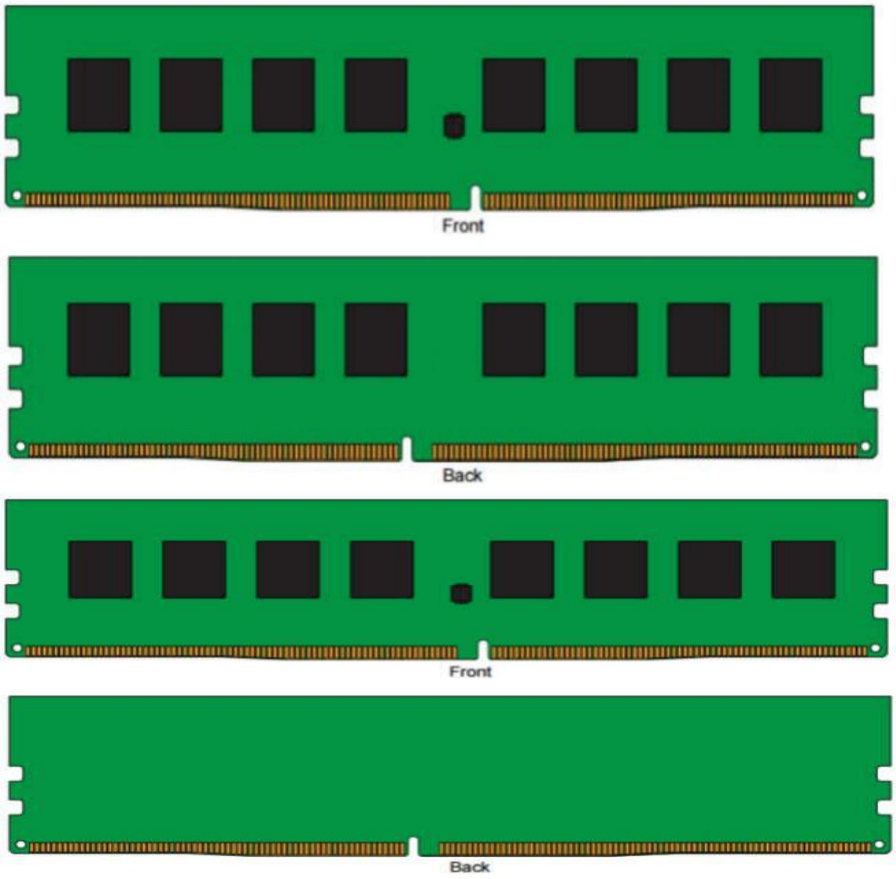
1.4.8 Serial presence detect with EEPROM;

1.4.9 Asynchronous reset;

1.4.10 Anti - sulfur resistor used;

2. Measurements

L133.35mm * W31.25mm * H4.0mm, Error±0.15mm (e.g. Figure 1)



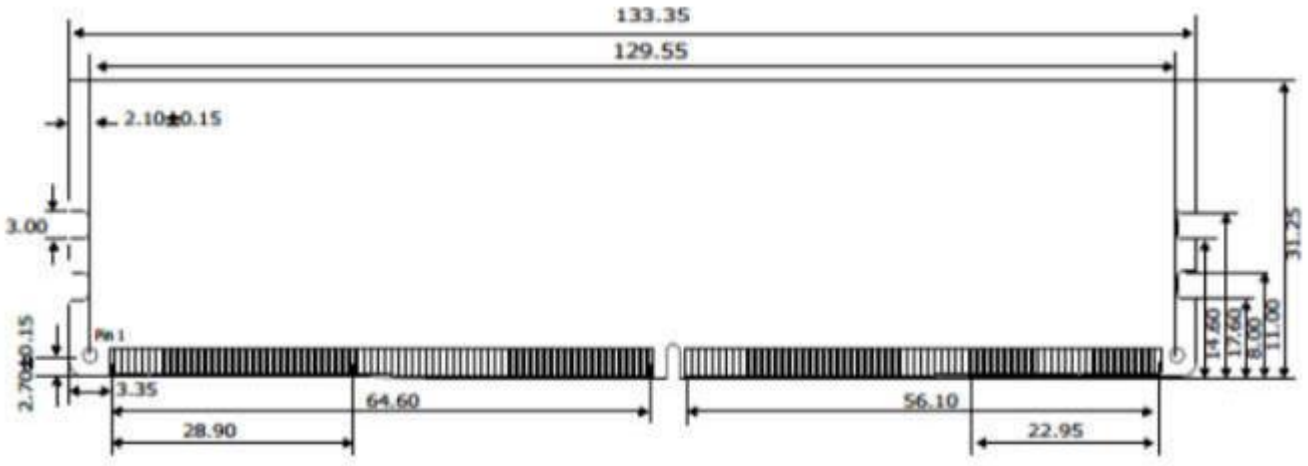


Figure 1

3 . Interface description/ Pin description

(e.g. Figure 2)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V	46	DQ20	91	CB1,NC	136	VDD	181	VSS	226	VSS
2	VSS	47	VSS	92	CB0,NC	137	CK0_t	182	DQ39	227	VSS
3	DQ5	48	VSS	93	VSS	138	CK1_t	183	DQ38	228	DQ50
4	DQ4	49	DQ17	94	VSS	139	CK0_c	184	VSS	229	DQ51
5	VSS	50	DQ16	95	DQS8_c	140	CK1_c	185	VSS	230	VSS
6	VSS	51	VSS	96	DM8_n/D BI8_n, NC	141	VDD	186	DQ35	231	VSS
7	DQ1	52	VSS	97	DQ S8_t	142	VDD	187	DQ34	232	DQ60
8	DQ0	53	DQ S2_c	98	VSS	143	PARITY	188	VSS	233	DQ61
9	VSS	54	DM2_n/D BI2_n, NC	99	VSS	144	A0	189	VSS	234	VSS
10	VSS	55	DQS2_t	100	CB6,NC	145	BA1	190	DQ45	235	VSS
11	DQ S0_c	56	VSS	101	CB2,NC	146	A10/AP	191	DQ44	236	DQ57
12	D M0_n/D BI0_n, NC	57	VSS	102	VSS	147	VDD	192	VSS	237	DQ56
13	DQS0_t	58	DQ22	103	VSS	148	VDD	193	VSS	238	VSS
14	VSS	59	DQ23	104	CB7,NC	149	CS0_n	194	DQ41	239	VSS
15	VSS	60	VSS	105	CB3,NC	150	BA0	195	DQ40	240	DQS7_ c
16	DQ6	61	VSS	106	VSS	151	A14/ WE_n	196	VSS	241	DM7_n / DBI7_n
17	DQ7	62	DQ18	107	VSS	152	A16/ RAS_n	197	VSS	242	DQS7_t
18	VSS	63	DQ19	108	RESET_n	153	VDD	198	DQS5_ c	243	VSS
19	VSS	64	VSS	109	CKE0	154	VDD	199	M5_n/ D BI5_n	244	VSS
20	DQ2	65	VSS	110	CKE1	155	ODT0	200	VSS	245	DQ62

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
21	DQ3	66	DQ28	111	VDD	156	A15/ CAS_n	201	VSS	246	DQ63
22	VSS	67	DQ29	112	VDD	157	CS1_n	202	VSS	247	VSS
23	VSS	68	VSS	113	BG1	158	A13	203	DQ46	248	VSS
24	DQ12	69	VSS	114	ACT_n	159	VDD	204	DQ47	249	DQ58
25	DQ13	70	DQ24	115	BG0	160	VDD	205	VSS	250	DQ59
26	VSS	71	DQ25	116	ALERT_n	161	ODT1	206	VSS	251	VSS
27	VSS	72	VSS	117	VDD	162	C0,CS 2_ n,NC	207	DQ42	252	VSS
28	DQ8	73	VSS	118	VDD	163	VDD	208	DQ43	253	SCL
29	DQ9	74	DQ S3_c	119	A12	164	VREFCA	209	VSS	254	SDA
30	VSS	75	DM3_n/D BI3_n, NC	120	A11	165	C1,CS 3_ n,NC	210	VSS	255	VDDSP D
31	VSS	76	DQ S3_t	121	A9	166	SA2	211	DQ52	256	SA0
32	DQ S1_c	77	VSS	122	A7	167	VSS	212	DQ53	257	VPP
33	DM1_n/ D BI1_n, NC	78	VSS	123	VSS	168	VSS	213	VSS	258	VTT
34	DQS1_t	79	DQ30	124	DQ54	169	DQ37	214	VSS	259	VPP
35	VSS	80	DQ31	125	VSS	170	DQ36	215	DQ49	260	SA1
36	VSS	81	VSS	126	DQ50	171	VSS	216	DQ48		
37	DQ15	82	VSS	127	VSS	172	VSS	217	VSS		
38	DQ14	83	DQ26	128	DQ60	173	DQ33	218	VSS		
39	VSS	84	DQ27	129	VDD	174	DQ32	219	DQS6_ c		
40	VSS	85	VSS	130	VDD	175	VSS	220	DM6_n / DBI6_n , NC		
41	DQ10	86	VSS	131	A3	176	VSS	221	DQS6_t		
42	DQ11	87	CB5, NC	132	A2	177	DQS4_c	222	VSS		
43	VSS	88	CB4, NC	133	A1	178	M4_n/ D BI4_n	223	VSS		
44	VSS	89	VSS	134	EVENT_n	179	DQS4_t	224	DQ54		
45	DQ21	90	VSS	135	VDD	180	VSS	225	DQ55		

Figure 2